CLAIMS

What is claimed is:

1. A system comprising:

a processor; and

a memory device coupled to the processor that comprises:

a memory array; and

a buffer device comprising:

a plurality of comparators, wherein each of the plurality of comparators is adapted to receive a data signal and one of a first signal and a second signal, wherein the second signal is a complimentary signal of the first signal; and

a plurality of two channel comparators adapted to receive a plurality of output signals from the plurality of comparators and to produce a first output signal and a second output signal with the second output signal being a complimentary signal of the first output signal.

2. The system, as set forth in claim 1, wherein the memory device comprises a dynamic random access memory.

3. The system, as set forth in claim 1, wherein the memory device comprises a static random access memory.

4. The system, as set forth in claim 1, wherein the processor is coupled to a communication port.

5. The system, as set forth in claim 1, wherein the processor is coupled to an input device.

6. The system, as set forth in claim 1, wherein the processor is coupled to a display.

7. The system, as set forth in claim 1, wherein the memory device comprises a pin adapted to receive the data signal.

8. The system, as set forth in claim 7, wherein the processor transmits the data signal through the pin to the buffer device.

9. The system, as set forth in claim 1, wherein the data signal comprises control information.

10. The system, as set forth in claim 1, wherein the data signal comprises address information.

11. The system, as set forth in claim 1, wherein each of the plurality of comparators comprises a differential amplifier.

12. The system, as set forth in claim 1, wherein each of the plurality of two channel comparators comprises a two channel differential amplifier.

13. The system, as set forth in claim 1, wherein the first signal is a clock signal.

14. An input buffer comprising:

a plurality of comparators, wherein each of the plurality of comparators is adapted to receive a data signal and one of a first signal and a second signal, wherein the second signal is a complimentary signal of the first signal; and

a plurality of two channel comparators adapted to receive a plurality of output signals from the plurality of comparators and to produce a first output signal and a second output signal with the second output signal being a complimentary signal of the first output signal.

15. The input buffer, as set forth in claim 14, wherein each of the plurality of comparators comprises a differential amplifier.

16. The input buffer, as set forth in claim 14, wherein each of the plurality of two channel comparators comprises a two channel differential amplifier.

17. The input buffer, as set forth in claim 14, wherein the data signal comprises control information.

18. The input buffer, as set forth in claim 14, wherein the data signal comprises address information.

19. The input buffer, as set forth in claim 14, wherein the plurality of comparators comprises:

a first comparator adapted to:

receive the data signal at a positive input terminal;

receive the first signal at a negative input terminal; and

produce a first comparator output signal;

a second comparator adapted to:

receive the data signal at a positive input terminal

receive the second signal at a negative input terminal; and

produce a second comparator output signal;

a third comparator adapted to:

receive the first signal at a positive input terminal

receive the data signal at a negative input terminal; and

produce a third comparator output signal; and

a fourth comparator adapted to:

receive the second signal at a positive input terminal

receive the data signal at a negative input terminal; and

produce a fourth comparator output signal.

20. The input buffer, as set forth in claim 19, wherein the plurality of two channel comparators comprises:

a first two-channel comparator adapted to:

receive the first comparator output signal at a first positive input terminal;

receive the second comparator output signal at a second positive input terminal;

receive the third comparator output signal at a first negative input terminal;

receive the fourth comparator output signal at a second negative input terminal; and

produce the first output signal; and

a second two-channel comparator adapted to:

receive the third comparator output signal at a first positive input terminal;

receive the fourth comparator output signal at a second positive input terminal;

receive the first comparator output signal at a first negative input terminal; and

receive the second comparator output signal at a second negative input terminal; and

produce the second output signal.

21. A memory device comprising:

a memory array;

a plurality of sense amplifiers coupled to the memory array; and

a buffer device couple to the memory array, the buffer device comprising:

a plurality of comparators, wherein each of the plurality of comparators is adapted to receive a data signal and one of a first signal and a second signal, wherein the second signal is a complimentary signal of the first signal; and

a plurality of two channel comparators adapted to receive a plurality of output signals from the plurality of comparators and to produce a first output signal and a second output signal with the second output signal being a complimentary signal of the first output signal.

22. The memory device, as set forth in claim 21, wherein the memory device is a dynamic random access memory device.

23. The memory device, as set forth in claim 21, wherein the memory device is a static random access memory device

24. The memory device, as set forth in claim 21, wherein the data signal comprises control information.

25. The memory device, as set forth in claim 21, wherein the data signal comprises address information.

26. The memory device, as set forth in claim 21, wherein the first signal is a clock signal.

27. The memory device, as set forth in claim 21, comprising a pin coupled to the buffer device for receiving the data signal.

28. The memory device, as set forth in claim 21, wherein each of the plurality of comparators is a differential amplifier.

29. The memory device, as set forth in claim 28, wherein each differential amplifier comprises:

a first input terminal coupled to a gate of a first transistor, the first transistor being coupled in series between a third transistor that is connected to a first voltage source and

a fourth transistor that is coupled to a second voltage source, wherein a gate of the fourth transistor is coupled to an enable signal;

a second input terminal coupled to a gate of a second transistor, the second transistor being coupled in series between a fifth transistor that is connected to a third voltage source and the fourth transistor, wherein a gate of the third transistor and the fifth transistor are coupled between the third transistor and the first transistor; and

an output terminal that is coupled between the second transistor and the fifth transistor.

30. The memory device, as set forth in claim 21, wherein each of the plurality of two channel comparators is a two channel differential amplifier.

31. The memory device, as set forth in claim 30, wherein each two channel differential amplifier comprises:

a first input terminal coupled to a gate of a first transistor, the first transistor being coupled in parallel with a second transistor;

a second input terminal coupled to a gate of the second transistor, the first transistor and the second transistor being coupled in series with a third transistor and a fourth transistor;

a third input terminal coupled to a gate of a fifth transistor, the fifth transistor being coupled in parallel with a sixth transistor;

a fourth input terminal coupled to a gate of the fourth transistor, the third transistor and the fourth transistor being coupled in series with the fourth transistor and a seventh transistor, wherein a gate of the third transistor and a gate of the seventh transistor are coupled between the first transistor, the second transistor and the third transistor;

a first enable terminal coupled to a gate of an eighth transistor, the eighth transistor being coupled in series between a first voltage source and the third transistor and the seventh transistor;

a second enable terminal coupled to a gate of the fourth transistor, the fourth transistor being coupled between a second voltage source and the first transistor, the second transistor, the fifth transistor, and the sixth transistor; and

an output terminal that is coupled between the fifth transistor, the sixth transistor and the seventh transistor.

32. A method of operating a buffer, the method comprising the acts of:

receiving a data signal at each of a plurality of comparators;

receiving one of a first signal and a second signal at each of the plurality of comparators, wherein the second signal is a complimentary signal of the first signal;

generating a respective one of a plurality of output signals from each of the plurality of comparators;

receiving each of the plurality of output signals at each of a plurality of two channel comparators;

generating a first output and a second output from the plurality of two channel comparators, wherein the second output signal is a complimentary signal of the first output signal.

33. The method, as set forth in claim 32, wherein the act of receiving the data signal comprises receiving control information.

34. The method, as set forth in claim 32, wherein the act of receiving the data signal comprises receiving address information.

35. The method, as set forth in claim 32, wherein the first signal is a clock signal.

36. The method, as set forth in claim 32, wherein each of the plurality of comparators comprises a differential amplifier.

37. The method, as set forth in claim 32, wherein each of the plurality of two channel comparators comprises a two channel differential amplifier.